

ANC0003

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Associated Application Notes: [ANC0001](#), [ANC0002](#), [AN1263](#)

Application Note Abstract

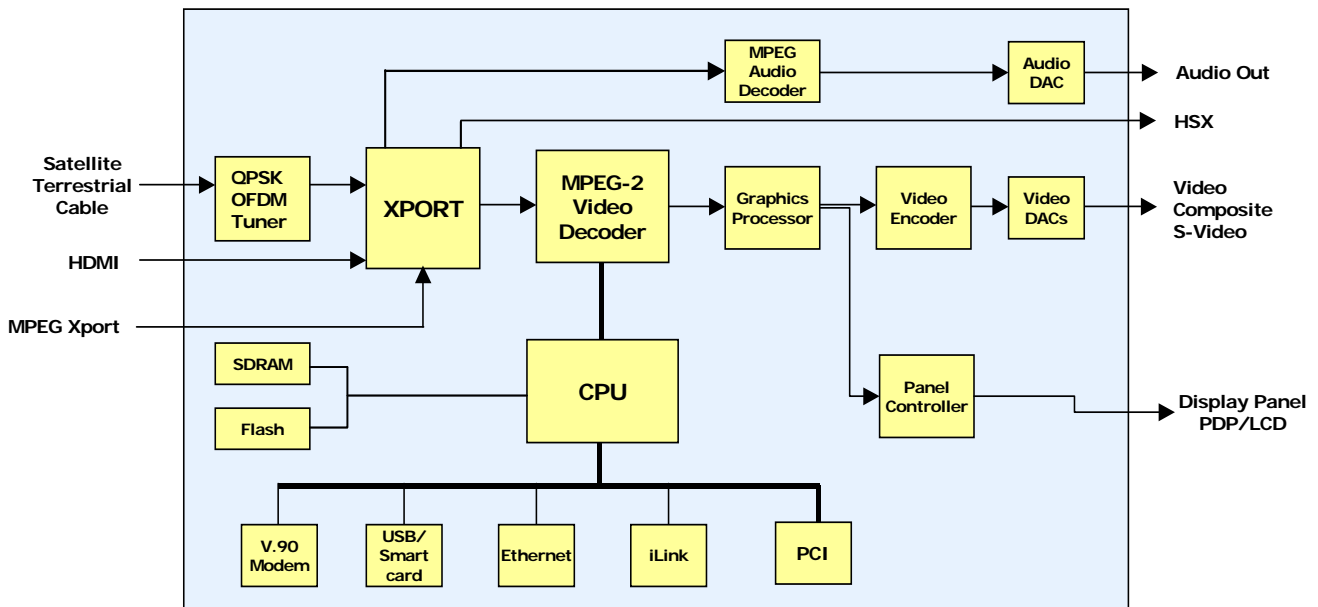
This document provides an overview of a standard DTV (digital television) system with regards to typical clock requirements. The discussion includes a list of the different clocks needed, frequency and performance requirements, signal integrity, and VCXO (voltage-controlled crystal oscillator) functionality as it relates to the DTV system.

This article addresses generic block diagrams, frequency usage and selection tables, critical requirements of the system, and an overview of Cypress-related clocking products to meet video system demands.

HDTV and STB Generic Block Diagram

From a black box viewpoint, the DTV/STB takes an incoming digital stream of data, which is processed in order to produce the appropriate format of video and audio output signals used by the television set. The following block diagram shows the main functional blocks; some of these components may be integrated into the ASIC/CPU in some cases.

Figure 1. Typical DTV Block Diagram

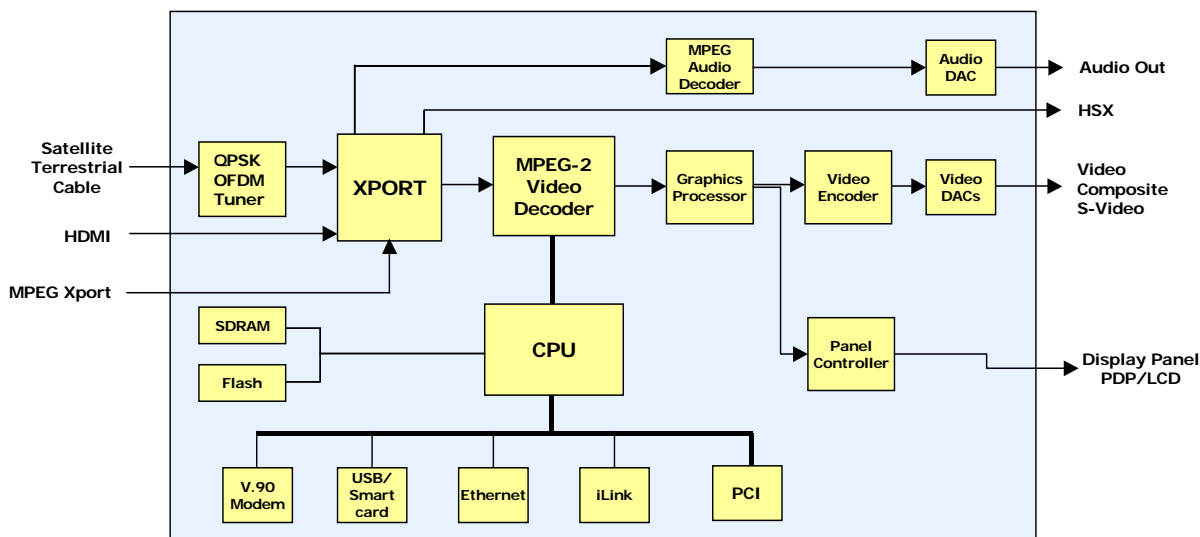


Several of the functional blocks shown in [Figure 1 on page 1](#) require a clock input. The CPU/ASIC system clock frequency can vary widely and may have several different requirements in terms of performance. This is also usually true for the graphics processor. Input clocks for the MPEG-2 video decoder, audio DAC, modem, USB, Ethernet, iLink, and PCI blocks usually follow the frequency standards used in their respective applications. The panel controller clock depends heavily on the display format/size. A more detailed discussion of clock requirements for each functional block can be found

in the [Critical Requirements](#) section on page 5 of this document.

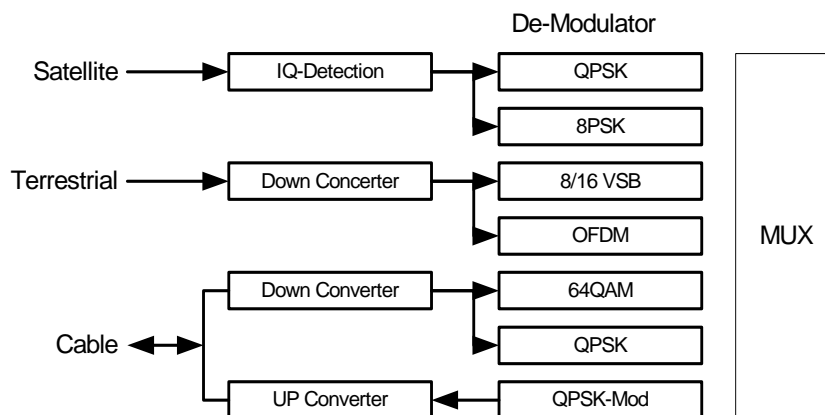
[Figure 2](#) shows an actual single-chip STB solution using an ASIC from Zoran. It includes all of the picture processing (including TS decoding) and audio decoding and outputs. USB, iLink, and HDMI interfaces are not shown on the diagram. The required clock outputs for the system are provided by the CY22388 4-PLL VCXO clock generator.

Figure 2. Example STB Block Diagram With Cypress Timing Solution



The RF tuner unit may be responsible for the functions shown in [Figure 3](#). Incoming RF-modulated data is converted to TS (Transport Stream) in the RF tuner unit and then sent to the ASIC. Note that modulation type and bandwidth requirements depend on the region and format.

Figure 3. RF Tuner Unit Block Diagram (All current formats)



Description of the Clocks

As seen from the block diagram shown in [Figure 1 on page 1](#), there are many functions required for DTV/STB applications; this section describes which clock frequencies are typically needed for each function.

Video Clocks

The video clocks are 27.000 MHz-based (27 MHz, 54 MHz, 81 MHz) and are used for the MPEG decoder. Because the decoder must be synchronized with the exact frequency used to encode the data, a VCXO is used in combination with the ASIC to match the output frequency to the reference source. An in-depth discussion of the use of a VCXO is presented in the section [Using a VCXO in a DTV System on page 8](#) of this document.

Audio Clocks

The clock frequencies used for audio in a DTV system are mainly for a DAC (digital-to-analog converter). The actual frequency can be determined based on the sampling frequency (F_s) and oversampling ratio. F_s formats include 32 kHz (miniDV, camcorders), 44.1 kHz (audio CDs, mp3s), and 48 kHz (digital TV, DVD, professional audio), while the oversampling ratio depends on the DAC and is usually 256, 384, 512 or 768. Based on these sampling rates and ratios, the most common audio frequencies can be calculated, shown in [Table 1](#) below.

Table 1. Audio clock Frequencies (in MHz) by Sampling Frequency and Oversampling Ratio

Oversampling ratio / F_s	32 kHz	44.1 kHz	48 kHz
256	8.192	11.2896	12.288
384	12.288	16.9344	18.432
512	16.384	22.5792	24.576
768	24.576	33.8688	36.864

It is important to note that audio clocks MUST have 0p pm synthesis error. This will be discussed further in the section [Using a VCXO in a DTV System on page 8](#) of this document.

USB Clock

48.00 MHz is typically used for a USB or Smart Card input clock.

Ethernet Clock

25.00 MHz is typically used.

iLink Clock

24.576 MHz is typically used.

Note that This is also an audio frequency.

Modem Clock

4.9152 MHz and 11.0592 MHz are commonly used frequencies, but ultimately the required frequency is dependent on the modem.

HDMI (Receiver for DTV / Transmitter for STB)

28.322 MHz is used for low-end models—in this case the 720 x 480 size is actually pseudo HD. True HD formats use video (display panel) frequencies, e.g. 74.25 MHz.

ASIC

As previously mentioned, the ASIC input frequency requirement varies, but is typically in the range of 30 MHz to 100 MHz. Some applications may require spread spectrum on the system clock for EMI reduction purposes.

PCI

33.3333 MHz is used, and spread spectrum is usually required. This is because most applications that need PCI will require multiple PCI clocks. The design may either use a “dual trace” to supply a single clock output to two destinations, or it may use a zero-delay buffer to supply the clock output to more than two destinations.

Display (Panel) Clock

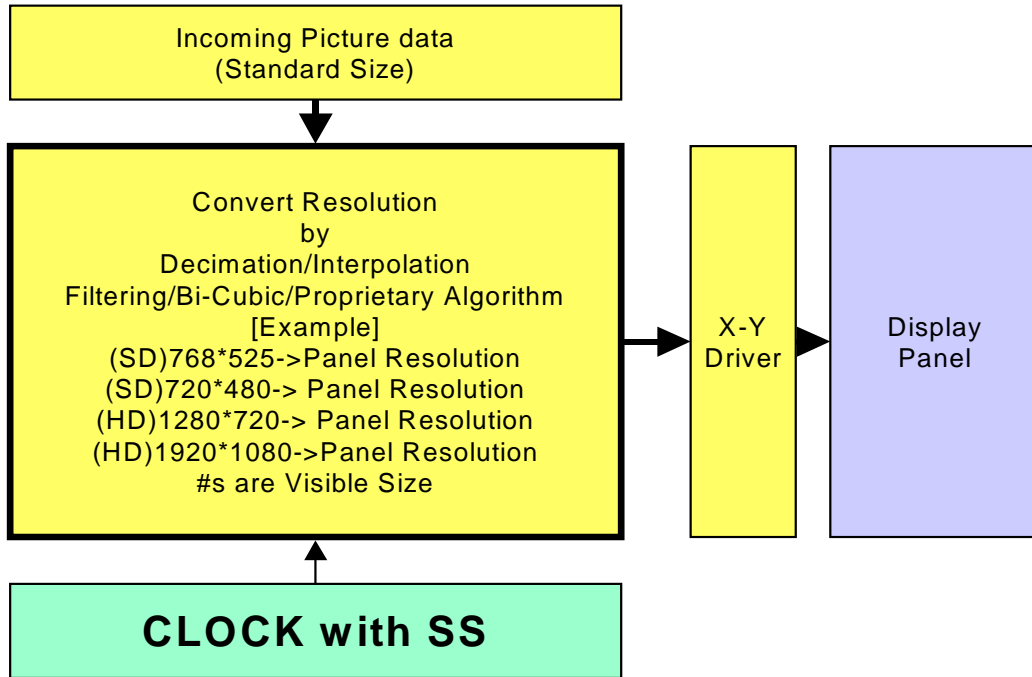
The panel clock frequency varies widely because it depends on the panel size (resolution). [Table 2](#) and [Table 3](#) show the relationship between frequency and panel size. The panel controller block diagram is shown in [Figure 4 on page 4](#). The primary function is changing picture size from the standard picture size to fit the actual panel screen size, as the incoming picture size and panel resolution are usually different (not a 1:1 ratio). For example, SD formats (768*525) displayed on an HD panel (1280*720) are not the true HD size.

The secondary function is color processing in conjunction with resizing the picture. Using proprietary algorithms, the incoming picture must be interpolated/decimated, color processed, HUE/SAT etc., and then all the pixel information must be shifted into the panel along with the reference clock.

The reference clock may be spread spectrum capable if the panel is PDP/LCD, because the location on the screen is addressed by X and Y clock position so there is no concern about ‘wrong’ positioning as there would be with an analog CRT.

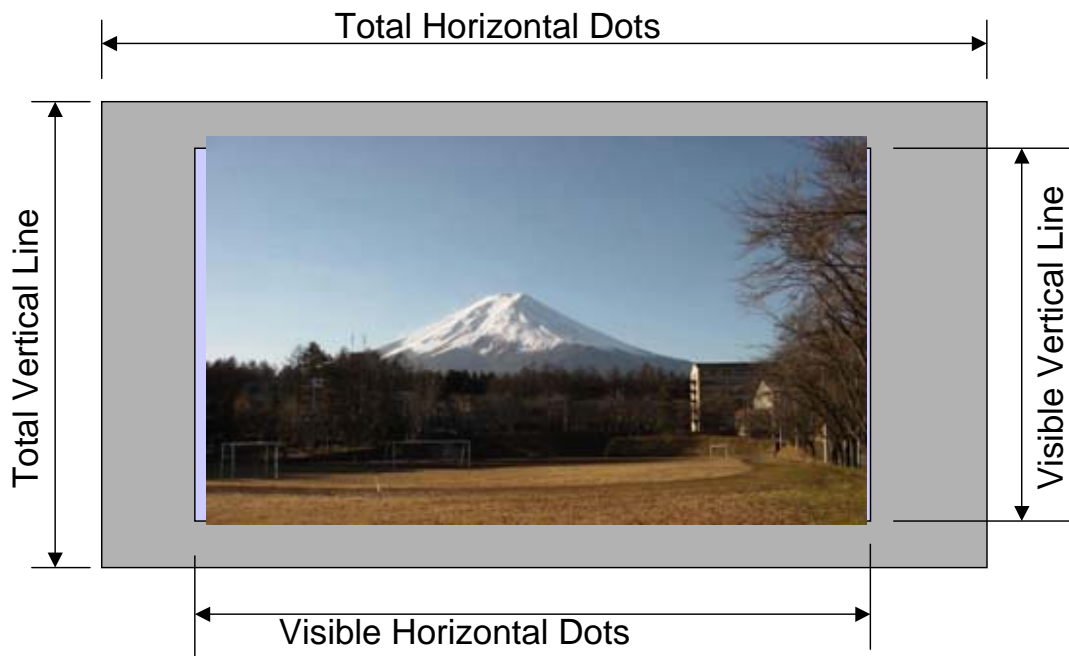
Figure 4 is a simplified block diagram.

Figure 4. Panel Controller Block Diagram



The display screen's horizontal and vertical size are shown in Figure 5.

Figure 5. Screen Size Description



The screen can be viewed in the visible horizontal and vertical size area, but the control clock frequency is only related to the total horizontal and vertical size. Therefore, the visible line data for the clock frequency calculation is not needed, but rather the total line data.

Table 2 shows the standard frequencies for the display panel clock, while Table 3 provides examples of customer specific requirements for varying panel sizes.

Table 2. SD and HD Standard Formats

Total H-Dots	Total V-Lines	Frame Rate (Hz) ^[1]	Frequency (MHz)	Comment
2200	1125	29.97	74.17582418	HD-1080i
2200	1125	30	74.25	HD-1080i
1980	750	50	74.25	HD-720p
910	525	29.97	14.31818181	SD-NTSC-4fs
858	525	29.97	13.5	SD-ITUR(NTSC)
1135	625	25	17.734375	SD-PAL-4fs
864	625	25	13.5	SD-UR(PAL)

Table 3. Proprietary Requirements by HD Frequency (depending on panel size)

Total H-Dots	Total V-Lines	Frame Rate (Hz) ^[1]	Frequency (MHz)	Comment
1186	562.5	59.94005994	39.9875124	
1186	1125	59.94005994	79.97502498	
1650	806	59.94005994	79.71428571	
1650	750	59.94005994	74.17582418	
2200	1125	59.94005994	74.17582418	HD Common F
1420	565	59.94005994	48.08991009	HD Common F

Other

Specific DTV systems may have additional features to distinguish them from the competition. Examples of possible applications that may require different frequencies include a game port, mass storage port, card interface, etc. These frequencies depend on their specifications. In Japan, DTV must have a so-called "B-CAS" card for ID recognition. In this case, Philips TDA8004 is generally used for the interface, requiring a 4 to 16 MHz clock.

Critical Requirements

This section describes the critical requirements for each clock application, including frequency accuracy and signal integrity.

Clock Frequency Accuracy

There are two types of clock frequency accuracy: absolute and relative. Absolute accuracy is critical when dealing with communication standards, such as USB or Ethernet, while relative accuracy is important for reference, video, and audio clocks. The accuracy for reference to video—27 MHz to 54 MHz, for example—should be 0 ppm; similarly, video to audio—54 MHz to 24.576 MHz, as another example—should also be 0 ppm. It is not always clear which type of clock accuracy is important, so it is important for the engineer to understand the system and applications to determine the

appropriate type of accuracy. Absolute and relative accuracy will be identical when a VCXO is locked to the incoming stream, assuming that the incoming data stream source (for example, a television studio, in the case of DTV) encoded the data with an absolute accuracy of 0 ppm.

Video Clocks

If the system has an analog (and/or D-terminal) video output, the clock must have 0 ppm synthesis error. In systems using a 74.17582418 MHz clock, there is a large counter inside the ASIC that counts clock edges to determine when the frame is complete. Therefore, if the clock has some non-zero ppm error, the picture frame will be corrupted. If the system has separate references for video-out and panel-clock, the panel-clock can have significant synthesis error and spread spectrum functionality as well.

Audio Clocks

Audio clocks must ALWAYS have 0 ppm synthesis error. In the MPEG-2/DVD digital stream, video is encoded based on 27 MHz and audio is encoded based on the 48 kHz sampling rate. Then the video and audio are synchronized to each other. Therefore, if the audio clock has non-zero synthesis error, the video and audio will not be synchronized successfully.

Note

1. $29.97 = 30 * 1000 / 1001$; $59.94005994 = 60 * 1000 / 1001$. The 1000:1001 ratio is used to convert to the true NTSC frame rate.

USB Clock

500 ppm synthesis error is acceptable per the standard but often system engineers will typically require ± 100 ppm

Ethernet Clock

± 100 ppm synthesis error is acceptable

iLink Clock

± 100 ppm synthesis error is acceptable

Modem Clock

± 100 ppm synthesis error is acceptable

HDMI

The HDMI interface clock should have 0 ppm synthesis error.

ASIC

This depends on the ASIC requirements; if spread spectrum is required, the acceptable error is in the order of percent.

PCI

Similar to ASIC clocks that use spread spectrum, percent order error may be acceptable.

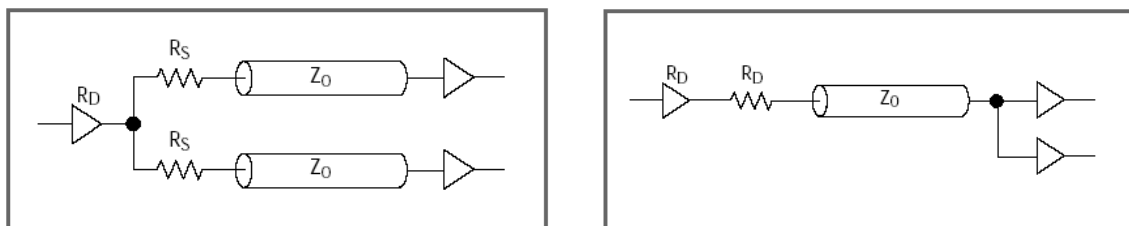
Signal Integrity

In any DTV design, the quality of clock signals is essential to ensuring proper system performance. If clock traces are not routed or terminated correctly, unwanted noise and reflections can degrade the edges. In some cases, poor signal integrity can lead to false triggers on a device input, often causing system failures. Clock edge integrity is an important part of system design.

For some particular frequencies in a DTV system, such as 27 MHz, 33.33 MHz, and some ASIC frequencies, two or more loads may be necessary. For more than two loads, the system design should use a zero-delay buffer or fan-out buffer. Problems arise due to reflections from each destination that degrade the signal integrity. A simulation of the design with an IBIS model in order to verify that the trace will perform as expected is also recommended. In some cases, the clock output drive strength may be adjusted through programming to better match the termination.

If a system design requires the multiple destinations but the designer does not wish to use a buffer—a buffer being the recommended solution—then the “dual trace” termination method is preferred over the “multiple loads” termination style. The circuits in Figure 6 below show the two methods, respectively.

Figure 6. Dual Trace and Multiple Loads



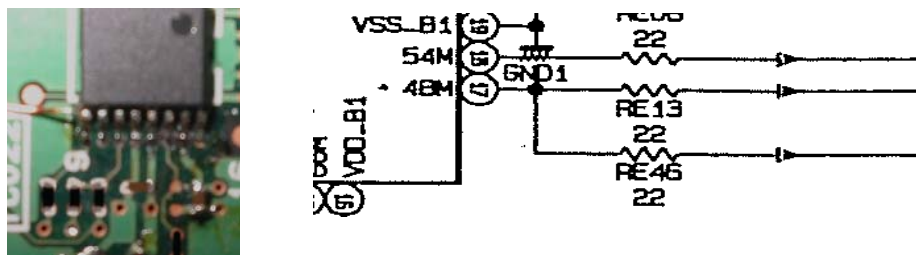
The “multiple loads” termination scheme is only useful if load conditions are the same and very close, and not much can be done regarding signal degradation due to reflections.

Another important aspect of the signal integrity of a clock is jitter. Excess jitter can rob a design of its precious cycle time or cause data to be latched incorrectly, or it can increase the noise floor of a DAC (digital-to-analog converter), degrading the SNR (signal-to-noise ratio).

For DTV systems, cycle-to-cycle jitter is important when driving an ASIC that has a downstream PLL inside. In this situation, problems may arise if the downstream PLL is unable to track the input frequency due to high absolute cycle-to-cycle jitter or high rate-of-change of cycle-to-cycle jitter. Clocks used for DTV system communications or analog signals (audio/video) are more affected by period and long-term jitter. Clock jitter requirements depend on the respective application and should be taken into account when designing a DTV clocking system.

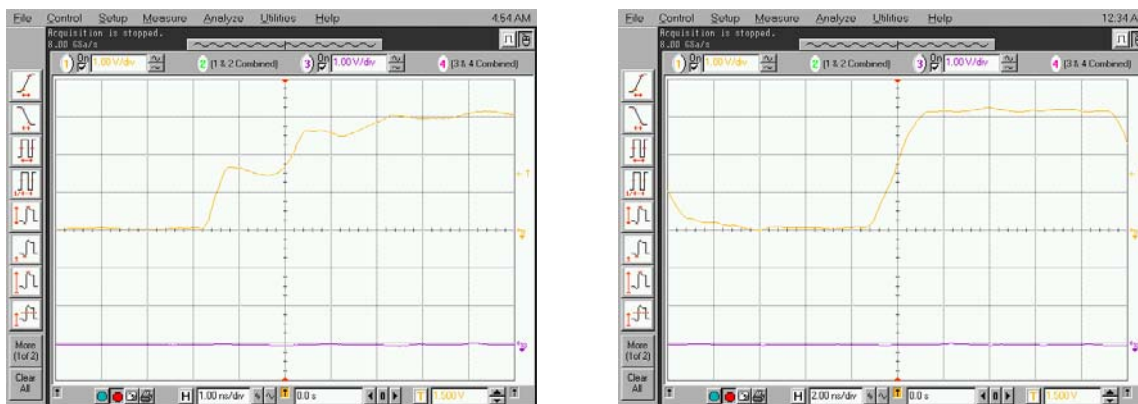
The following photo, schematic, and oscilloscope captures show how poor system design can lead to clock signal integrity issues. In the photo and schematic of a clock generator in a DTV system, the “dual trace” method is used to drive two destinations with a single clock output.

Figure 7. Photo and Schematic of a Dual-Trace in an Actual System Board



Using this configuration, a system failure occurred due to a corrupt clock input signal. The left side of Figure 8 below shows a non-monotonic rising clock edge due to the use of the “dual trace” method with improper termination.

Figure 8. Improperly Terminated Clock Waveform (left), Properly Terminated Clock Waveform (right)



As seen from the scope capture, the kinks around the threshold voltage clearly cause problems for the DTV system. In this case, the root cause of the issue was a mismatched series termination. This can be solved either by reducing the value of the damping resistor or increasing the drive strength of the clock output, if possible. After changing the damping resistor (and choosing the proper clock output drive strength), the waveform was clean and monotonic, and the system failure was eliminated. In the case of increasing the drive strength of the clock output, the output impedance decreases while edge rates become faster. In some cases, this may raise the EMI generated by the output.

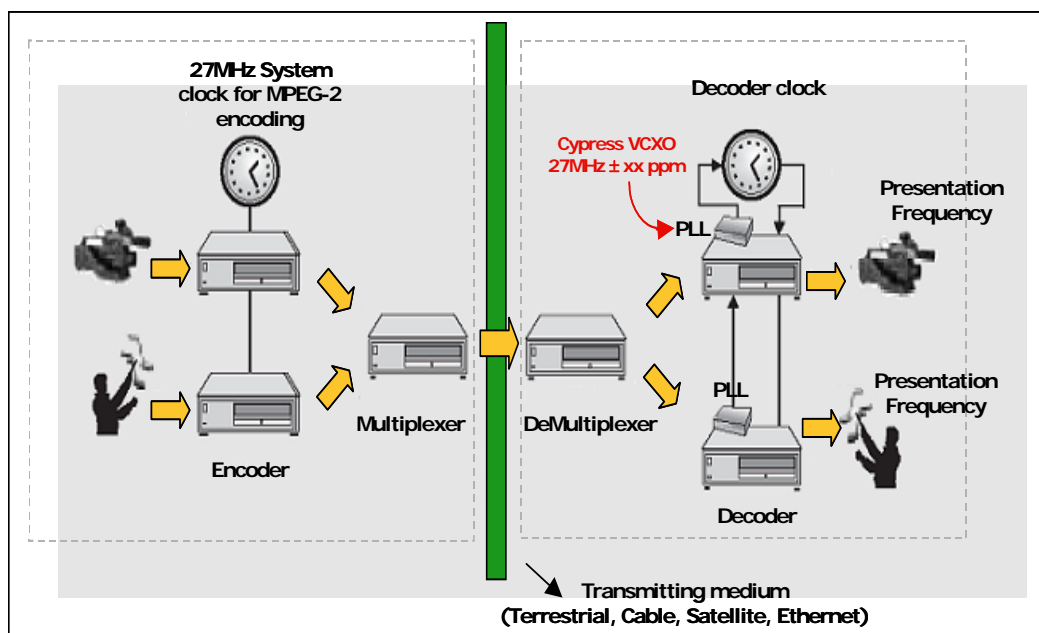
A key to designing a board with good clock integrity is to simulate the signals prior to manufacturing using IBIS models. Cypress provides IBIS models of the output buffers for all of its programmable clock products, including models for the different programmable drive strength levels.

Using a VCXO in a DTV System

This section describes the VCXO (Voltage-Controlled Xtal Oscillator), how it functions in the system, and the parameter requirements for the crystal and VCXO to operate properly.

An outline of how a VCXO works within the DTV system is shown in Figure 9.

Figure 9. MPEG-2 Encoding and Decoding Diagram



When encoding video for transmission, as is done at a TV studio, the encoding frequency is stamped into the digital stream, which is then transmitted via satellite, cable, or terrestrial broadcasting media. By definition, the time tolerance will be ± 32 ppm at the receiving end. At the receiver side, such as a DTV/STB, there is a local oscillator that must tune the local frequency to track the incoming stream. If the frequencies are not matched, the picture may be corrupted by under/over flow. In order to match the local frequency to the original encoding frequency, a VCXO is used. A VCXO is different from a regular crystal oscillator in two key ways. First, the oscillator circuit includes varactors that control the reac-

tive loading seen by the crystal, based on the V_{in} voltage fed back from the ASIC. Second, a different kind of crystal is used in VCXO applications. The VCXO crystal is selected in order to meet the pulling requirements of the application without causing excessive third harmonic coupling. For a detailed discussion on these effects, refer to a technical article published by Cypress titled "Design and Development Considerations of Voltage Controlled Crystal Oscillator (VCXO) Networks". A VCXO can be used to "tune" the local frequency to match the frequency that was used to encode the received video data stream. The crystal can be pulled to the nominal frequency by adding or subtracting external capacitance.

Figure 10. Fundamental Pull Circuit (VCXO)

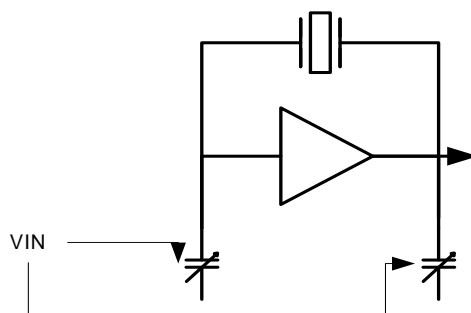
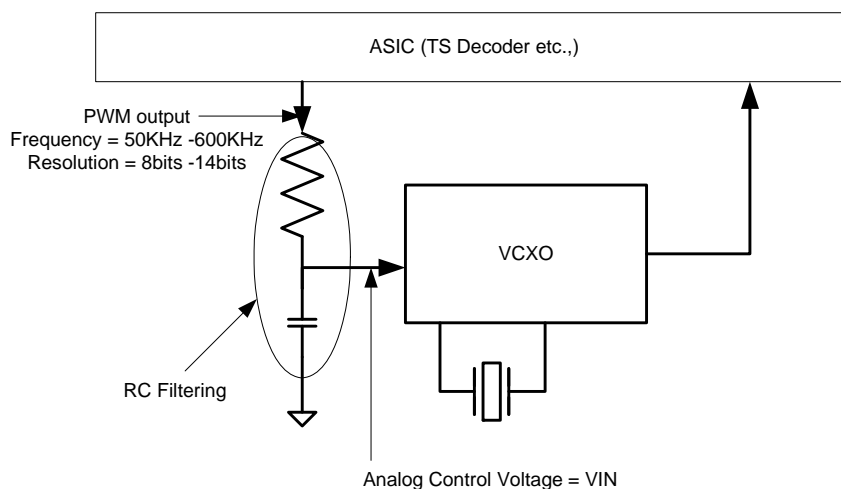


Figure 11 shows how the VCXO circuit works in the application. There is an error detector inside the ASIC that monitors the difference in frequency between the incoming stream and the local frequency through demodulation and carrier alignment. The amount of error is reflected in the PWM (Pulse Width Modulation) output and is used to provide feedback to the VCXO via the Vin pin. Thus the VCXO is able to tune the local frequency to match variations in the incoming stream, provided that the pull range is large enough to account for the amount of error between the signals, as the case would be in a well-designed system. An RC filter is usually used to convert the PWM signal to an analog control voltage. The resolution of the PWM is typically 8 to 14 bits.

Figure 11. VCXO Control Voltage Feedback Loop Diagram



The pull range of the VCXO is primarily dependent on the crystal, as can be seen from the equation in Figure 12.

Note Pull is defined by C0, C1, and CL only.

Figure 12. Frequency Pull Formula

$$PPM = \frac{C1 \times \left[\left(\frac{1}{C0 + Cxtal} \right) - \frac{1}{(C0 + CL)} \right] \times 10^6}{2}$$

Table 4 shows the margin and tolerances for the pull range for a DTV system.

Table 4. Pull Range PPM Components

MPEG-2	Acceptable ppm error as specified in the standards	±32 ppm
Crystal	Temperature coefficient	±20 ppm
Crystal	Initial accuracy	±20 ppm
Clock	Clock chip variations	±30 ppm
	Total	±102 ppm
	Total with ~20% Margin	±120 ppm

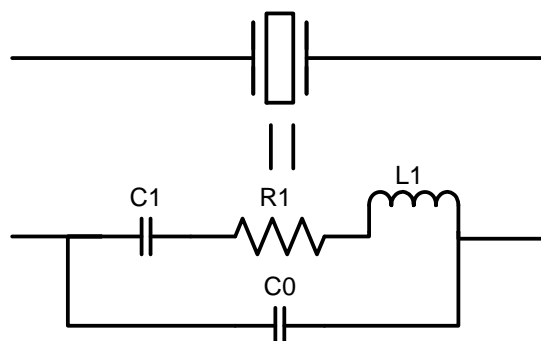
As shown in Table 4, systems typically require a pull range of ±120 ppm for a given crystal in order to be able to meet the needs of the DTV system with some design margin.

In older VCXO circuit designs, a large (HC-49/U) crystal was used, but as system boards have become smaller, crystals with smaller profiles are now used. 5032 (5.00 mm x 3.2 mm) size SMD type crystals are gaining in popularity in current designs. The parameters of the crystal depend on the crystal blank and electrode design. Thus, C0 and C1 decrease and ESR increases as the packages decrease in size. The pictures in Figure 13 on page 10 show the difference between crystals. Figure 14 on page 10 shows the crystal equivalent circuit.

Figure 13. Comparison of Crystal Packages



Figure 14. Crystal Equivalent Circuit



Parameter Descriptions

C0: Motional Capacitance, $C0 = k * \epsilon * (A/e)$

C1: Shunt Capacitance, $C1 = (8 * A * \epsilon^2) / (\pi * e * c)$

Where:

A = Electrode area

ϵ = Piezo-electric constant

e = Blank Thickness

k = Dielectric constant

c = Stiffness coefficient

Other Known Parameters

CL: Nominal frequency capacitive load

ESR (R1): Equivalent Series Resistance

Negative Resistance (-R)

As a rule of thumb: blank thickness (mm) = 1.67/freq (MHz).
For example, 13.5 MHz = 0.124 mm, 27 MHz = 0.062 mm

Negative resistance is the term given to the gain provided by an active device in an oscillator circuit to overcome losses and sustain oscillation. A primary component of circuit loss is the resistance of the quartz crystal. Crystal manufacturers specify this resistance in their crystal data sheets. The dominant failure mode for an oscillator circuit with low negative R or high crystal resistance is the oscillator failing to start when power is applied to the circuit.

Spurious signals can cause problems in any VCXO system, including DTV systems. Frequency “jumping” often occurs if there is an overlap between the third electrical harmonic and the mechanical third harmonic. To prevent this, the system designer should specify mechanical third overtone range either above or below the electrical third overtone range. For more information, please refer to the Cypress technical article “Design and Development Considerations of Voltage Controlled Crystal Oscillator (VCXO) Networks.”

Table 5. Example of a Crystal Specification

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
F_nom	Nominal Frequency	Parallel resonance, AT cut, fundamental mode		27		MHz
F_delta25	Frequency Tolerance	at 25°C	-20		+20	ppm
F_deltaT	Temperature Tolerance	0-70°C (referenced to 25°C)	-20		+20	ppm
CL_nom	Nominal Load Capacitance			12		pF
R1	Equivalent Series Resistance	Fundamental mode (CL = series)		20	50	Ohms
DL	Drive Level	Nominal VDD at 25°C			500	μΩ
C0	Shunt Capacitance		1.8	2.0	2.3	pF
C1	Motional Capacitance		6.4	7.1	8.3	fF
F3_sepHi	Third Overtone Separation from 3F0	Mechanical third (High side of 3F0)	240			ppm
F3_sepLo	Third Overtone Separation from 3F0	Mechanical third (Low side of 3F0)			-240	ppm

The most important parameters are: C0-Max, C1-Min-Max, DL-Max (Drive Level), and a definition that the mechanical third overtone and its associated in harmonic spurs be located outside the entire pull range of the electrical third harmonic. If this the last requirement is not met, the VCXO may have frequency 'jumps' or frequency 'bumps' or both at some points in the pull curve. You can tell whether or not a crystal

may have these problems by sweeping the capacitance values (via the Vin pin voltage) and accurately measuring the output frequency using a frequency counter. The following figure and Figure 16 on page 12 show such sweeps, revealing examples of a frequency 'bump' and a frequency 'jump', respectively.

Figure 15. VCXO Sweep Showing Frequency 'Bump'

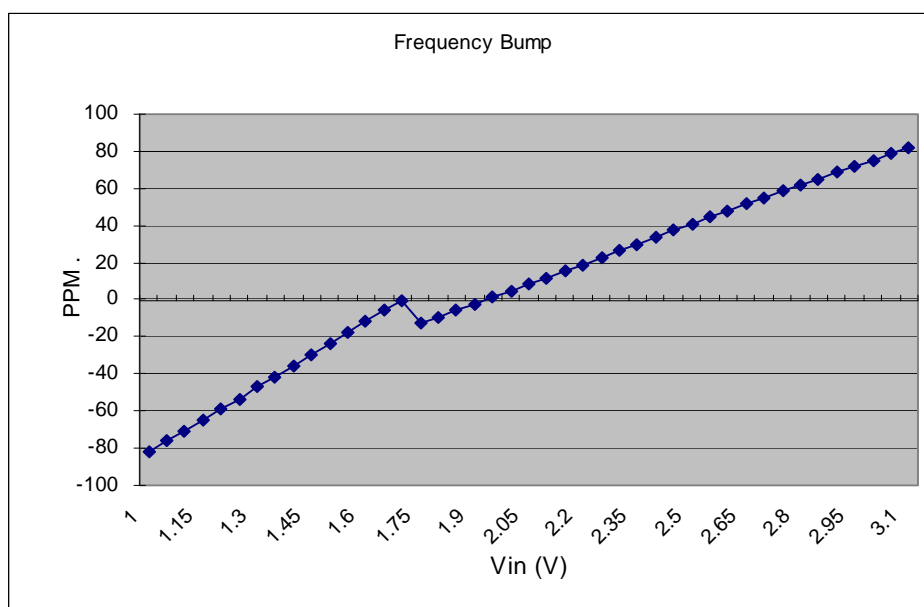
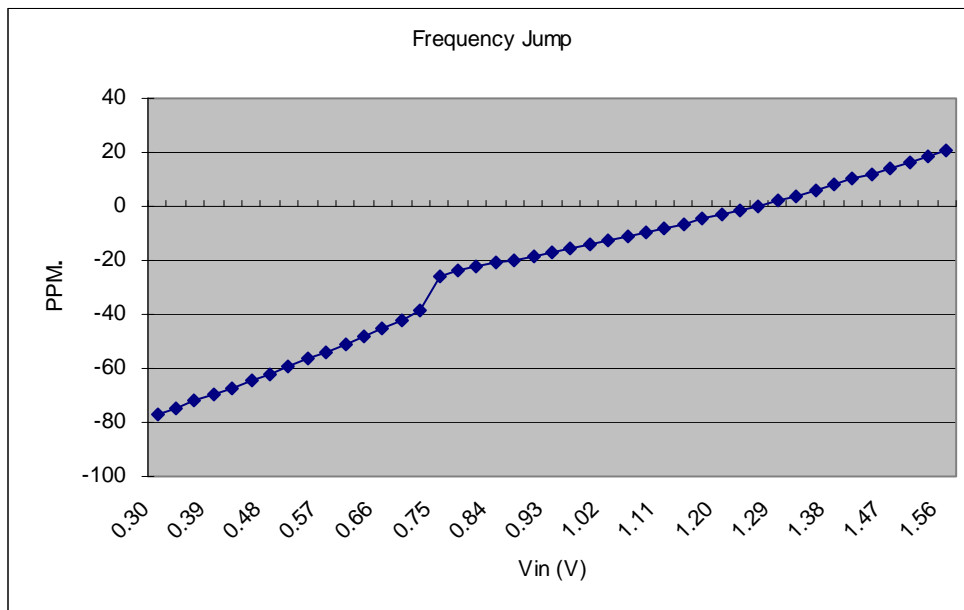


Figure 16. VCXO Sweep Showing Frequency 'Jump'



Cypress Timing Solutions

Cypress has a product family specifically designed to meet the timing needs of a digital TV system. The CY22388/CY22389/CY22391/CY24488 programmable clock series offers four PLLs with a VCXO and up to nine different outputs. The CY24488 offers I²C programming option. It has up to five outputs. In addition, the Cypress timing product portfolio includes numerous devices to meet other system needs, such as EMI reduction (for example, the CY25100 Programmable Spread Spectrum Clock Generator) or clock fanout (for example, the CY2305/CY2309 Clock Buffer family).

Finding the Right Solution


During the initial DTV design discussion, the system designer needs to consider all clock requirements. For example:

1. What frequencies are needed?
2. How many independent frequencies?
3. How many copies of each output frequency?
4. What kind of performance is required (jitter, spectral content, etc.)

The list of requirements could look something like this:

Total Clock Requirement

- Dual Tuner (Dual VCXO)
- Multiple ASICs
- Ethernet/USB/iLink
- Modem/Card
- HD-Size Panel
- Audio Clocks
- Etc., etc.,



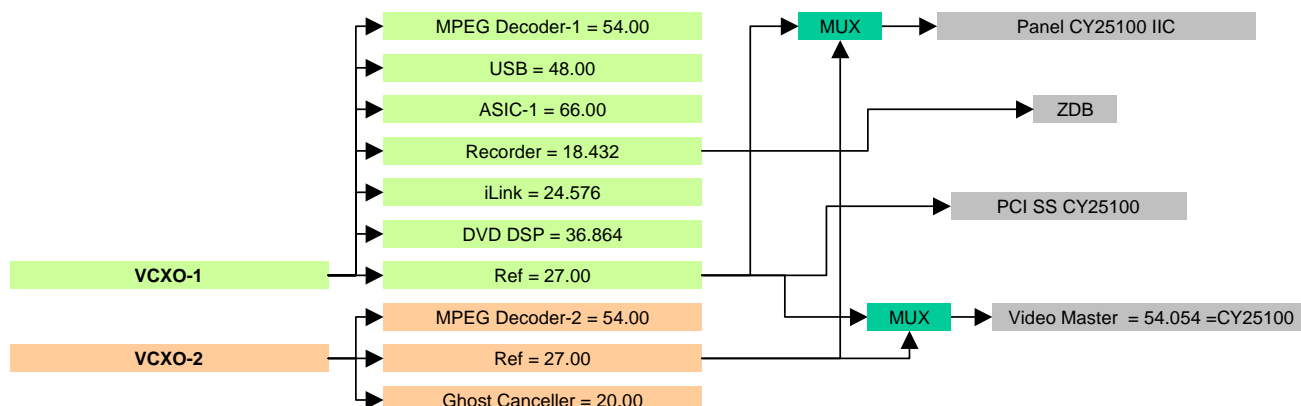
Next, more detailed information should be obtained, such as:

- Multiple Panel Clocks = 74.1758 etc.
- Video Master Clock = 54.054
- MPEG Decoder-1 = 54.00
- MPEG Decoder-2 = 54.00
- USB = 48.00
- ASIC-1 = 66.00
- Recorder = 18.432 * 4
- iLink = 24.576
- DVD DSP = 36.864
- PCI = 33.3333 SS
- Ref = 27.00 * 2
- Ghost Canceller = 20.00
- Dual VCXO**



Once the specific clock requirements are determined, an outline of the timing solution can be created.

Figure 17. Timing Solution Outline For Dual Tuner DTV Application

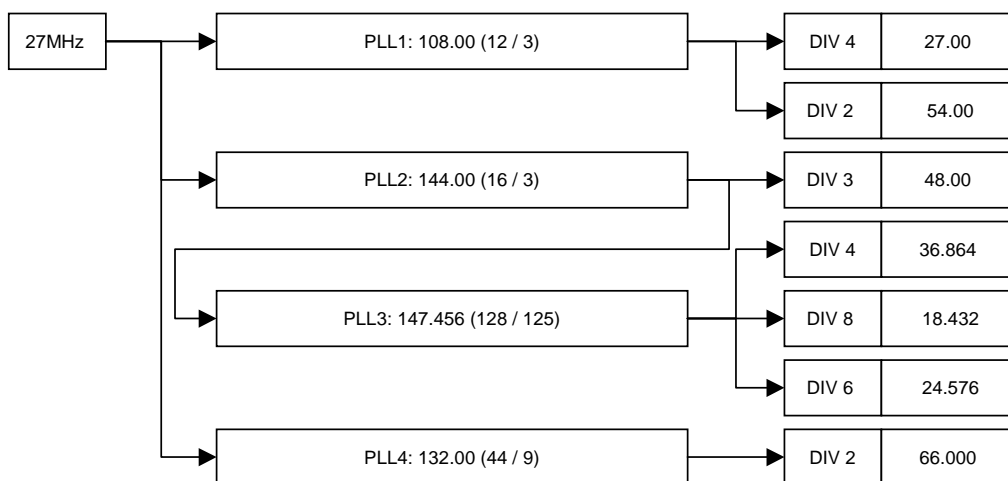


The example system in Figure 17 shows a clocking solution using two discrete CY22388 series clock generators and two multiplexers for a dual tuner DTV application. Many systems require EMI reduction on certain clock outputs—in the example above, the PCI clock requires spread spectrum functionality. In these cases, the CY25100 Programmable Spread Spectrum Clock Generator can be added to the design to provide the necessary spread. Additionally, a special option of the CY25100 can be used to generate the multiple panel clock frequencies, either via input frequency select pins or I2C programming. Zero delay buffers such as the

CY2305/CY2309 series are added in systems where a clock output frequency may need to be fanned out to several inputs.

In order to generate the many clock frequencies that derive from VCXO-1 (shown in green) in Figure 17, the device configuration shown in Figure 18 may be used. Note that in order to generate the audio frequencies from a 27 MHz reference, PLL cascading must be used in order to have 0 ppm synthesis error.

Figure 18. CY22389 PLL Configuration For Dual Tuner DTV Application



Using and Configuring the CY22388 Device Family

The CY22388 programmable device series is extremely flexible in the different timing solutions it can provide. However, this can make configuring the device somewhat confusing. This section describes the many features and capabilities of the CY22388 family of clocks and provides sample solutions and common configurations to help simplify the design-in process for a digital TV system.

Available Features

Predictable Output Phase Relationship

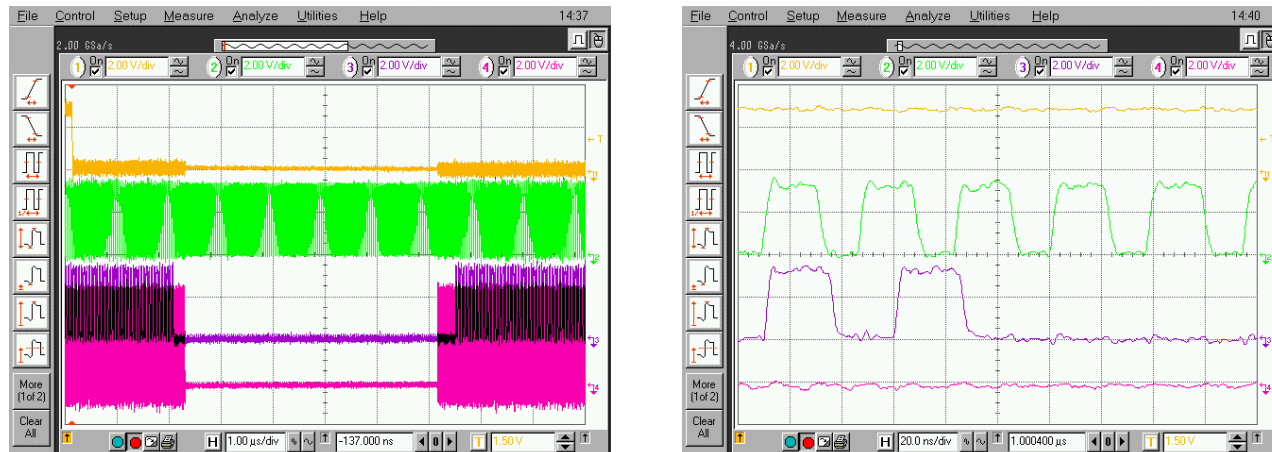
Depending on clock output divider design, clock outputs that are binary multiples deriving from the same PLL still may not have a predictable phase relationship upon power up. However, the CY22388/CY22389/CY22391/CY24488 series device guarantees predictable phase between such outputs. The device has an output synchronizing circuit inside that always aligns the output signals. There are two stages of output dividers: in the first stage, the PLL output is divided by 2 or by 3. In the second stage, the first stage outputs are fed to a divide-by 1, 2, 3, or 5 circuit. Thus, the total set of possible output divider values is {1,2,3,4,(5),6,8,9,10,12,15}. Note that the divide by 5 circuit is a bit different from others. If you

select the divide by 5, the first divider will necessarily be bypassed. As a result of this, output divider configuration, div-by-2 and div-by-3 outputs are ahead in phase when compared to divide values that require both stages.

Glitch-Free Output Multiplexer

As the audio clock frequencies change with the incoming audio format (for example, 44.1K [CDDA] to 48K [DVD/MPEG-2]) dynamically, a popping noise may occur due to the glitch while changing from one frequency to another. In the worst cases, the subsequent processing (DSP) may be hung up by the glitch (or by a higher frequency clock above its limitation). With many clock solutions, the burden lies with the system designer to devise a way to handle this issue, for example, muting the output audio and/or gating the clock for the DAC for the necessary time until the newly selected frequency is available. The CY22388 series has a special function called GFM (Glitch Free Mux) which drives the clock LOW on the falling edge of the current cycle during frequency select, then after a certain period, the output will be activated naturally with a rising edge at the proper newly selected frequency. For this device family the customer does not need to be concerned with glitches during frequency selection. An example of the GFM function is shown in [Figure 19](#).

Figure 19. Glitch-Free Mux Oscilloscope Shot (Left) and Close View (Right)



Low Voltage Output Capability

The CY22388 family has three different power supply domains: Core AVdd, Vdd Bank A, and Vdd Bank B. AVDD is used for the core power supply and must be 3.0V to 3.6V. Vdd Bank A supplies the CLK A, B, C and H output drivers. Vdd Bank B supplies the CLK D, E, F, and G output drivers. The output supplies support 2.5V operation in addition to 3.3V.

PLL Cascading

The data sheet for the CY22388 family does not explicitly mention the PLL cascading capability, but this feature does

exist and may be used to generate 0-ppm synthesis error frequencies that would otherwise be unavailable due to P/Q and/or PFD frequency limitations.

Programmable Tuning of Output Drive Strength and Duty Cycle

As mentioned during the signal integrity discussion, the CY22388 family has the capability of selecting among four different output drive strength settings to optimize performance within the system. Likewise, output duty cycle can be tuned over a limited range using I²C programming in order to optimize systems where the duty cycle requirement is critical.

Common Configurations

Most DTV systems have similar basic frequency needs. This section provides sample configurations that provide the most commonly used frequencies.

Video and Audio Frequencies

Common frequencies and possible P & Q PLL divider values are listed in [Table 6](#) and [Table 7](#).

Table 6. Video-related PLL Frequencies.

Video Frequency	Ref	Q	P	VCO	Div	Comment
74.25	27	2	11	148.5	2	
	27	4	33	222.75	3	
74.17582418	27	91	500	148.3516484	2	
	27	91	750	222.527472	3	
54.00	27	3	12	108	2	
	27	2	12	162	3	
	27	2	16	216	4	
54.054	148.5	125	182	216.216	4	
	99	125	273	216.216	4	
	27	125	1001	216.216	4	Use Charge Pump setting = 010

Table 7. Audio-related PLL Frequencies

Video Frequency	Ref	Q	P	VCO	Div	Comment
48K,32K series						
6.144				73.728	12	
12.288				73.728	6	
18.432				73.728	4	
24.576				73.728	3	
36.864				73.728	2	
44.1K series						
9.8304				147.456	15	
12.288				147.456	12	
16.384				147.456	9	
18.432				147.456	8	
24.576				147.456	6	
36.864				147.456	4	
44.1K series						
11.2896				135.4752	12	
16.9344				135.4752	8	
22.5792				135.4752	6	
33.8688				135.4752	4	
44.1K series						
11.2896				169.344	15	
16.9344				169.344	10	
33.8688				169.344	5	
44.1K series						
11.2896				101.6064	9	
16.9344				101.6064	6	
33.8688				101.6064	3	

Note that these audio frequencies cannot be generated from a single PLL when using a 27 MHz reference, so two PLLs must be cascaded. As mentioned earlier, a VCO frequency of 169.344 MHz can be generated from 108 MHz (multiple of 54) with 0 ppm synthesis error. Since the ratio of 44.1K and 48K is 147:160, the 44.1K series and the 48K series of frequencies can be easily generated from each other by cascading the PLLs and using a P/Q ratio of 147:160 or 160:147.

Modem

11.0592 MHz is a commonly used frequency and can be generated using P and Q values of (27 MHz reference) * 512 / 125 = 110.592 MHz, with 0 ppm synthesis error. However, because of the low phase detector frequency (27/125 = 216 KHz) of this configuration, a charge pump setting of CP = 010 should be used.

Ethernet

A 25 MHz output is typically generated from 100 or 200 MHz (or other) PLL frequency divided by 4 or 8, respectively. The 100 or 200 MHz PLL can also be used to generate the PCI clock frequency of 33.333 MHz.

USB

Normally a 48 MHz clock is used for USB, which is independent from other common frequencies, so a dedicated PLL will be needed for generating this frequency. Possible PLL frequencies include 96, 144, 192 and 240 MHz.

PCI

As mentioned in the Ethernet clock description, the same PLL that generates 25 MHz can be used to generate the 33.333 MHz required for PCI. In some consumer applications, customers may require 33.00 MHz instead of the 33.333 (=100/3) for safety margin, If so, a dedicated PLL would be needed for this clock. However, since 33.00 MHz is derived from 99.00 MHz (divide by 3), if a 54.054 MHz output for video is required, the 99 MHz PLL can be cascaded to a 216.216 MHz PLL that generates a 54.054 MHz output without any synthesis error (0 ppm).

iLink

A 24.576 MHz clock is used for iLink, which is identical to the audio clock frequency discussed previously.

Sample Configuration Diagrams

Figure 20. CY22388 PLL Configuration For DTV Application w/ 54 MHz output

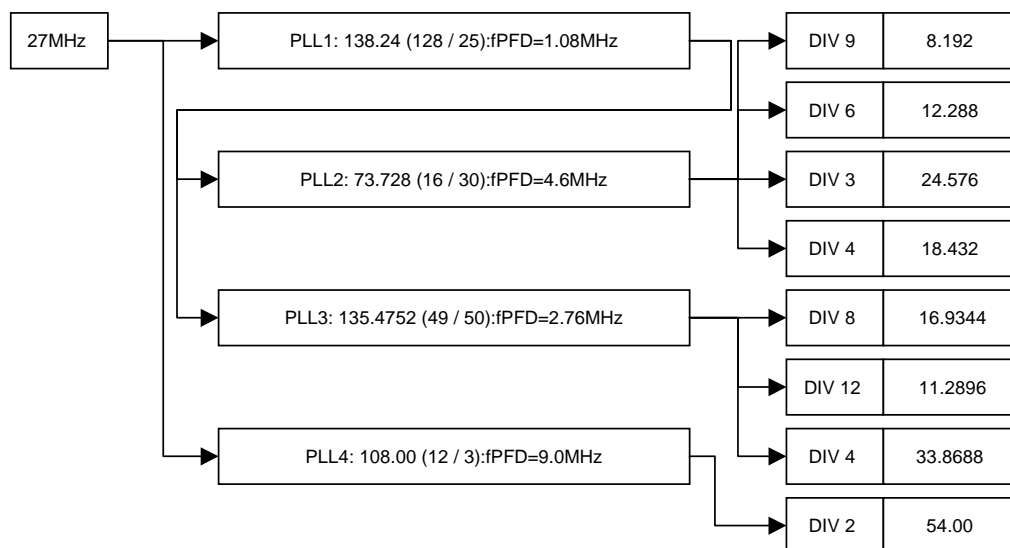


Figure 21. CY22388 PLL Configuration For DTV Application w/ 74.175824 MHz video clock output

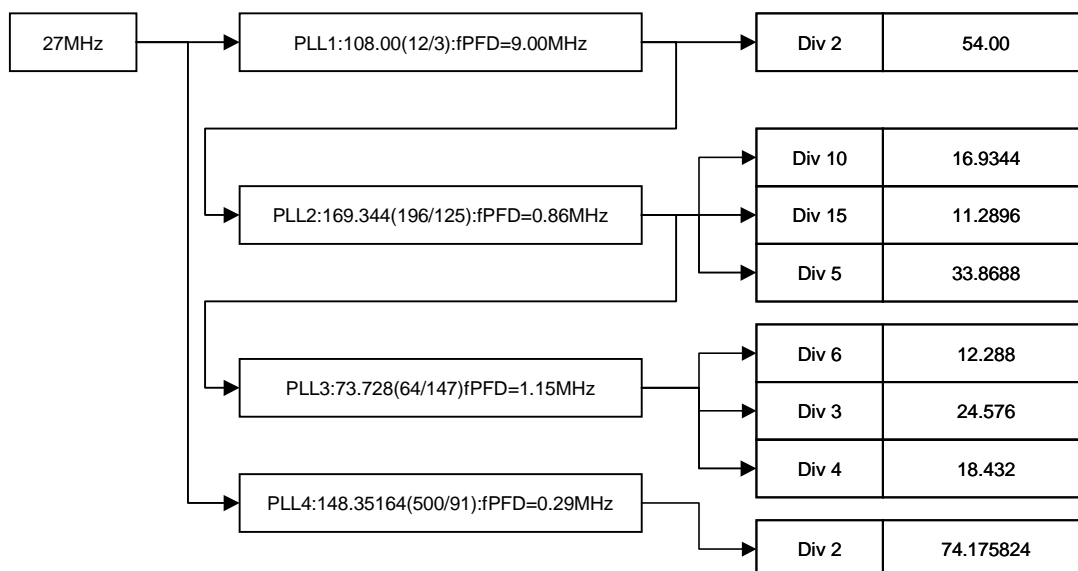
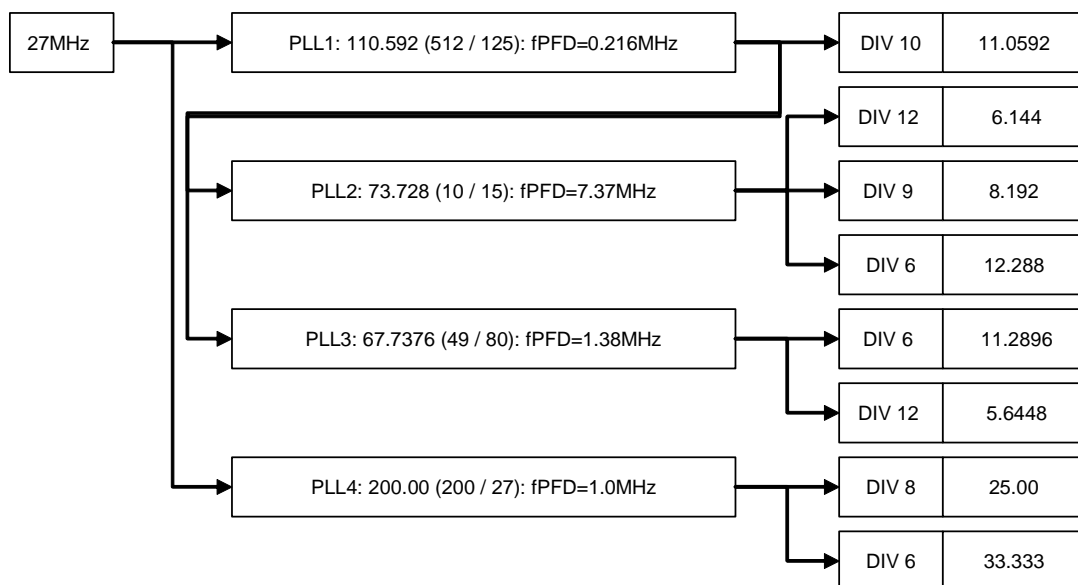


Figure 22. CY22388 PLL Configuration For DTV Application w/ 11.0592 MHz modem clock output



As can be seen from these configurations, most of the audio clock frequencies can derive from the same PLL, depending on the PLL frequency chosen. The output divider value can be changed to obtain the required audio clock.

Spread Spectrum and EMI Reduction

Due to FCC (or similar governing bodies) regulations to prevent EMI (electro-magnetic interference), the amount of energy radiated from a system at a given RF frequency is limited. Clock distribution is a major source of EMI in most systems.

In the past, the issue of EMI was usually resolved by shielding and/or reducing energy at the frequencies in question. This method, while often effective, could be costly and time consuming. A simple method to address system clock signals with excessive energy radiation is through frequency modulation, or 'spread spectrum'. In systems that can handle a small amount (often in the range of 0.5% to 5%) of frequency deviation, the energy can be spread out across a narrow frequency band, thus reducing the peak radiation at the center frequency and all of its harmonics. Spread spectrum is used in most personal computers today and is a cost-effective, versatile way to manage EMI reduction in any system.

Cypress provides a wide portfolio of products offering spread spectrum EMI reduction, including the programmable CY25100 Spread Spectrum PLL Clock Generator. For more information on spread spectrum and available products, please visit the Cypress home page at the link listed below.

Summary

While designing timing solutions for digital TV systems may be complicated, Cypress offers products that greatly simplify the process. The CY22388 4-PLL VCXO Clock Generator family can provide several independent output clock frequencies from a single crystal, allowing the system designer to save on cost, space, and complexity. Other clock products, including spread spectrum generators and zero-delay buffers, allow Cypress to offer a complete timing solution for any DTV system. For further information regarding Cypress timing products, visit <http://www.cypress.com> or contact your local Cypress field application engineer.

References

[AN1263](#) "Design and Development Considerations of Voltage Controlled Crystal Oscillator (VCXO) Networks"

[ANC0002](#) "CY22388 Application Note"

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